Amendments to the Claims

1. (PREVIOUSLY PRESENTED) A fuse for integration within a semiconductor circuit comprising: an insulating layer deposited adjacent the semiconductor substrate; a silicon layer formed a first silicon material having a first resistance deposited adjacent the insulating layer, the silicon layer having a first width; and, a metal silicide stringer having a second resistance different from the first resistance deposited over a portion of the first silicon material and having a second width that is less than the first width within at least a portion thereof, the metal silicide for conducting current therethrough with approximately the second resistance and for agglomerating in response to a programming current to other than conduct current therethrough with a same second resistance.

2. (ORIGINAL) The fuse as recited in claim 1 wherein the silicon layer is a poly-silicon layer.

3. (ORIGINAL) The fuse as recited in claim 1 wherein the silicide layer is a tungsten silicide layer.

4. (ORIGINAL) The fuse as recited in claim 1 wherein the silicide layer is a platinum silicide layer.

5. (ORIGINAL) The fuse as recited in claim 1 wherein the first resistance is higher than the second resistance.

6. (ORIGINAL) The resistor fuse as recited in claim 1 wherein the resistor fuse forms a portion of a non-volatile multi-state memory cell.

7. (ORIGINAL) The resistor fuse as recited in claim 6 wherein the memory cell is one-time programmable.

8. (ORIGINAL) The resistor fuse as recited in claim 1 wherein the insulating layer comprises an oxide layer.

9. (PREVIOUSLY PRESENTED) A method of manufacturing a silicided polysilicon fuse comprising the steps of: depositing an insulating layer on a semiconductor substrate; depositing polysilicon adjacent the insulating layer; forming a silicide protection layer adjacent the polysilicon; removing a portion of the silicide protection layer to reveal polysilicon therebelow; providing a mask for masking other than the revealed polysilicon; aligning the mask with the semiconductor substrate; and, forming a metal silicide layer adjacent the revealed polysilicon, the metal silicide layer for forming a conductive path along a length thereof.

10. (PREVIOUSLY PRESENTED) A method according to claim 9 comprising the step of providing electrical contacts on opposite sides of the length of the metal silicide layer.

11. (ORIGINAL) A method according to claim 9 wherein the insulating layer comprises an oxide layer.

12. (ORIGINAL) A method according to claim 9 wherein the polysilicon layer is patterned.

13. (ORIGINAL) A method according to claim 9 wherein the step of forming a silicide protection layer is performed by depositing a silicide protection layer on the polysilicon.

14. (ORIGINAL) A method according to claim 9 wherein the step of forming a silicide protection layer is performed by reacting at least a chemical with the polysilicon.

15. (ORIGINAL) A method according to claim 9 wherein the step of removing a portion of the silicide protection layer comprises a step of etching a portion of the silicide protection layer.

16. (ORIGINAL) A method according to claim 9 forming a metal silicide layer comprises a step of: depositing a metal silicide adjacent the revealed polysilicon.

17. (ORIGINAL) A method according to claim 9 forming a metal silicide layer comprises a step of: reacting at least a chemical including a metal with the revealed polysilicon.

Claims 18 – 20 (CANCELLED)

Claim 21 (CANCELLED)